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(54) Semiconductor integrated circuit interconnections

(57) A first signal line A_1, a second signal line B_0 and a third signal line A_2 are formed on a substrate 1 of a semiconductor integrated circuit. The effective distance $1_{A_1B_0}$ between the first signal line and the second signal line is substantially equal with the effective distance $1_{A_2B_0}$ between the second signal line and the third signal line.

The first signal line transmits a first signal e_1. The third signal line transmits a third signal $-e_1$ of which the phase is opposite to that of the first signal.

Thus, the cross talk from the first signal line to the second signal line can be cancelled by the cross talk from the third signal line to the second signal line.

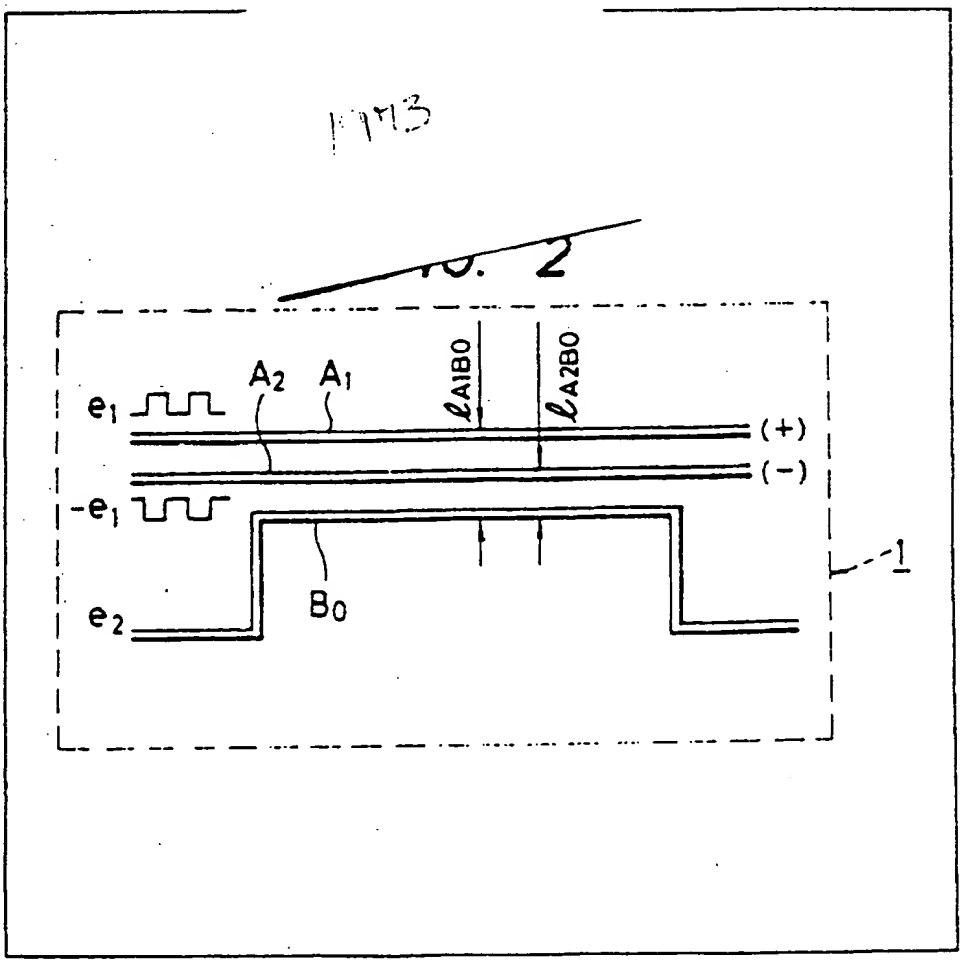

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FIG. 1

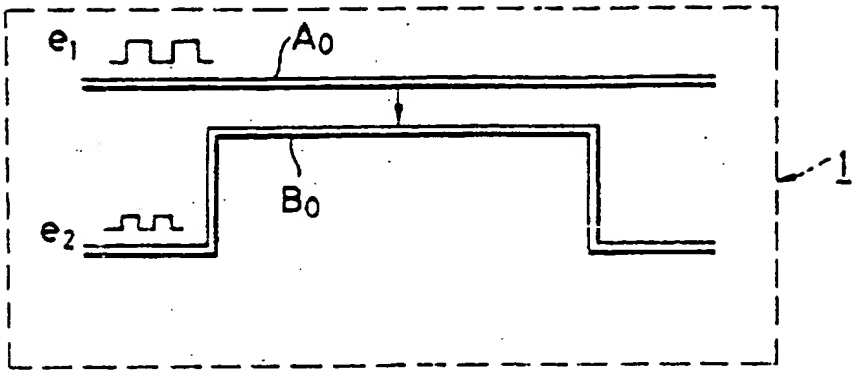


FIG. 2

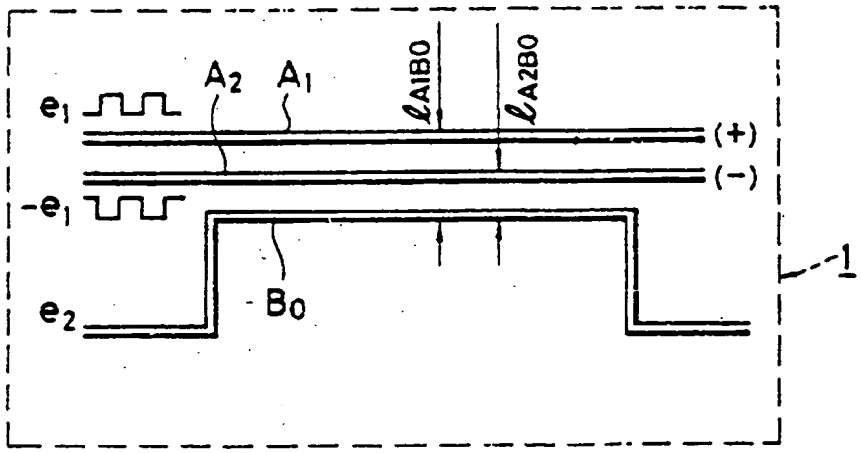


FIG. 3

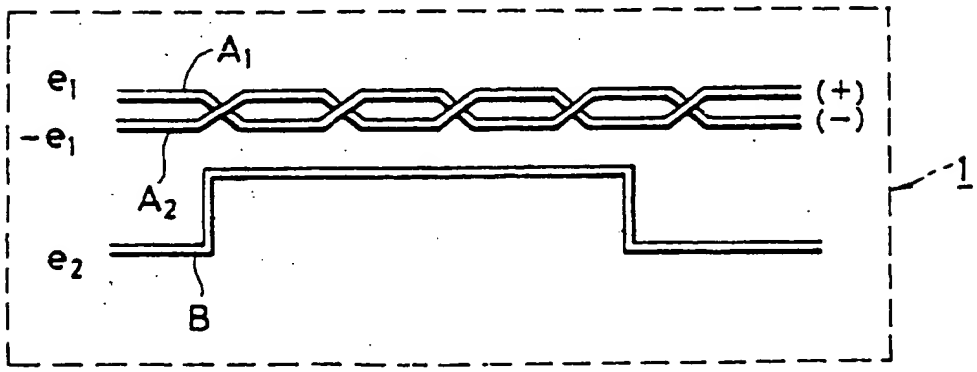


FIG. 4

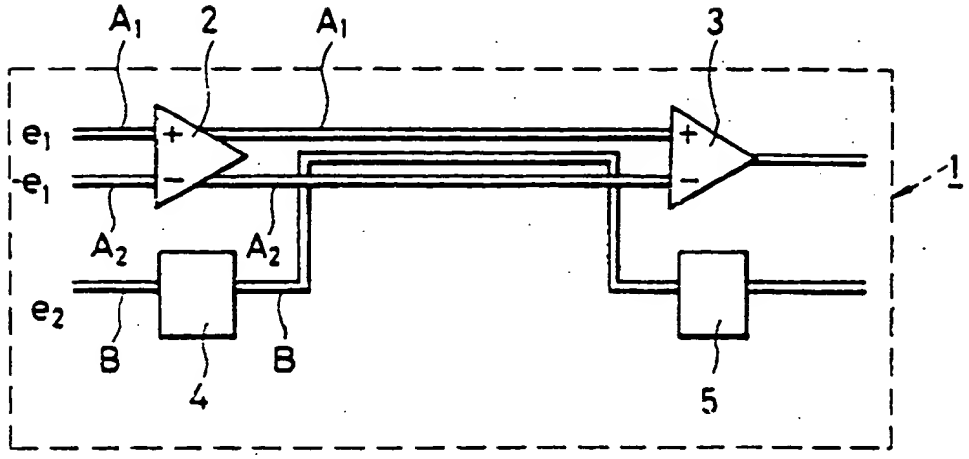


FIG. 5

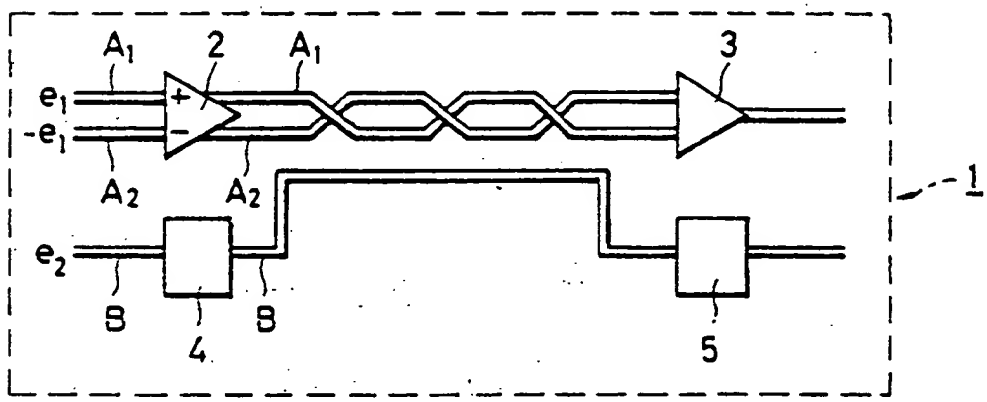


FIG. 6 (A)

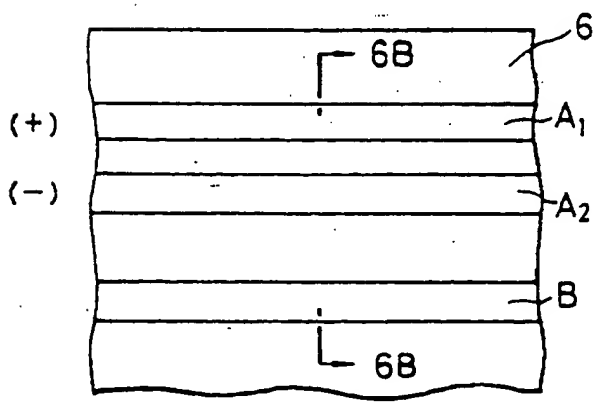


FIG. 6 (B)

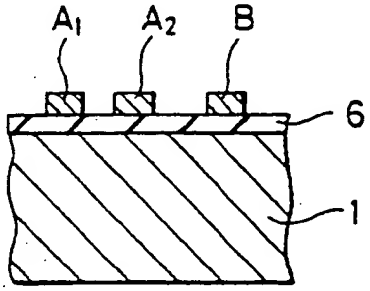


FIG. 7 (A)

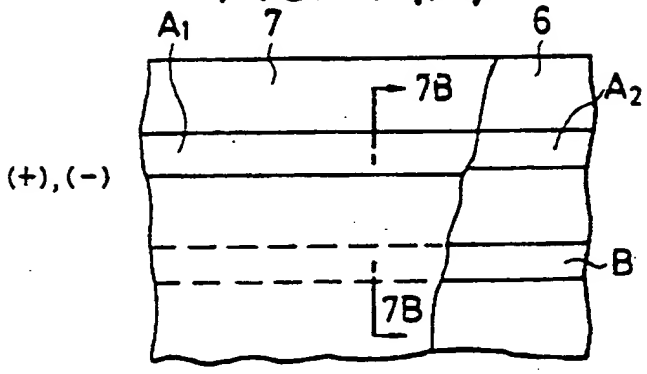


FIG. 7 (B)

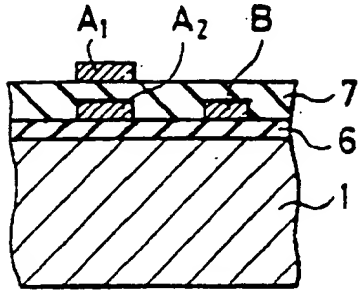


FIG. 8 (A)

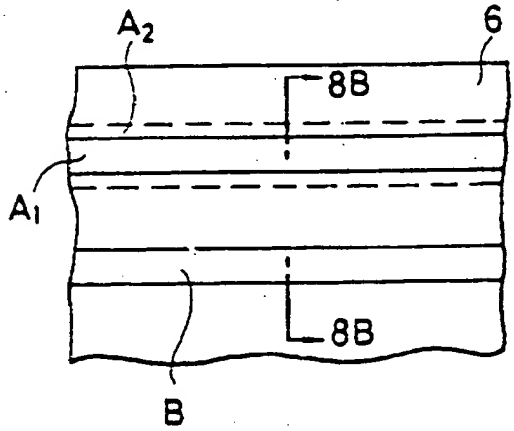


FIG. 8 (B)

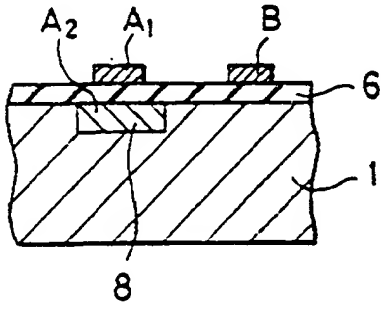


FIG. 9 (A)

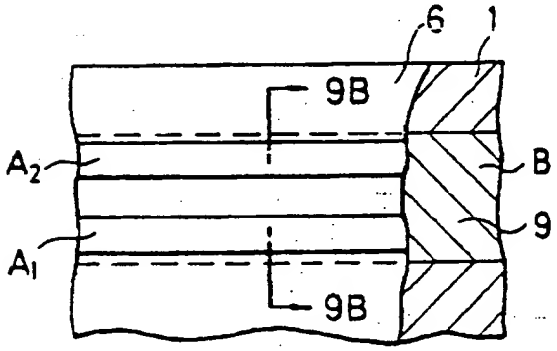


FIG. 9 (B)

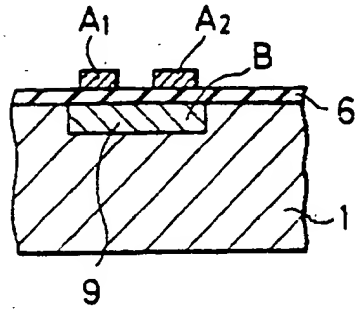


FIG. 10 (A)

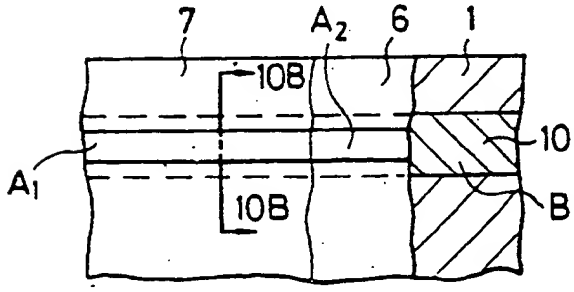


FIG. 10 (B)

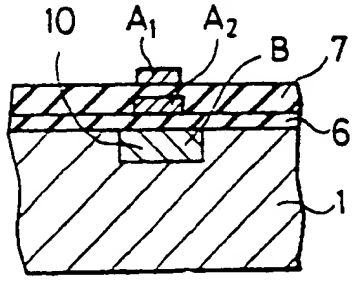


FIG. 11 (A)

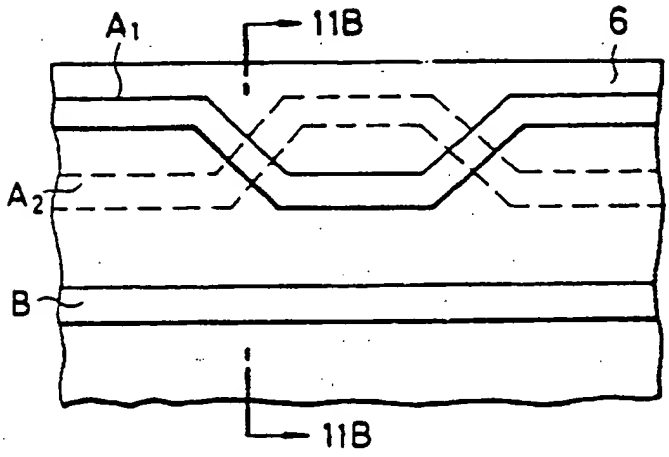


FIG. 11 (B)

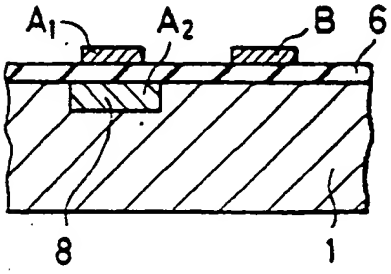


FIG. 11 (C)

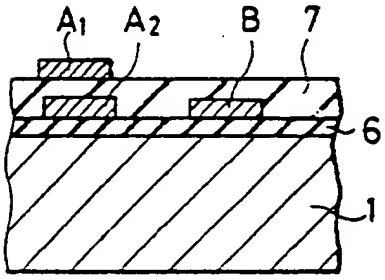


FIG. 12 (A)

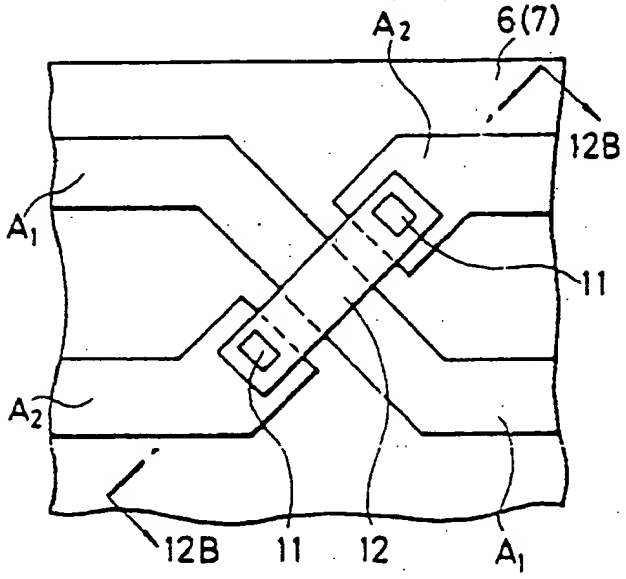


FIG. 12 (B)

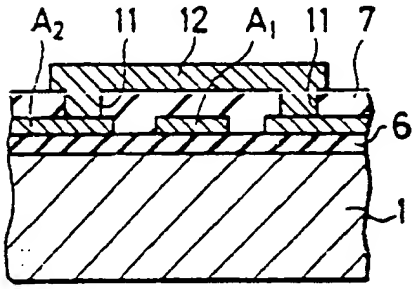


FIG. 13 (A)

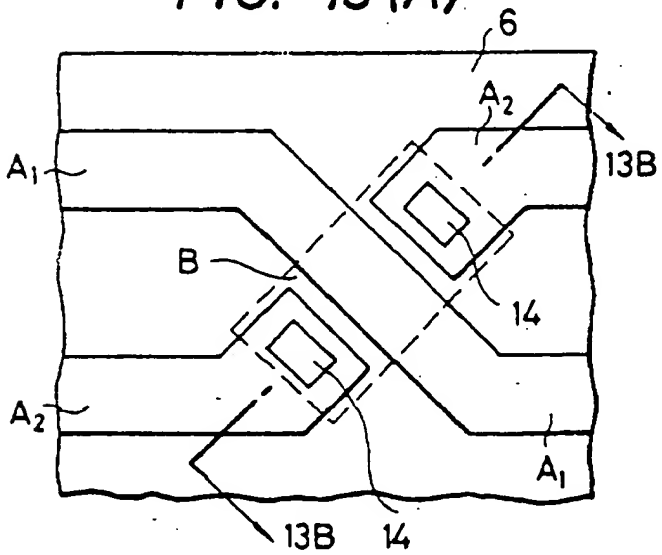
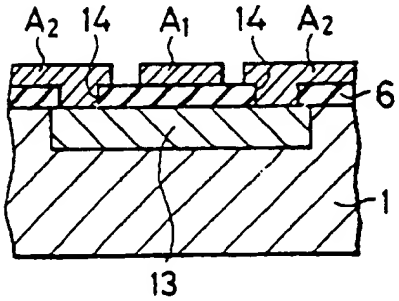


FIG. 13 (B)



SPECIFICATION

Semiconductor integrated circuit

The present invention relates to a semiconductor integrated circuit and seeks to reduce interference between signal lines thereof.

In a semiconductor integrated circuit which processes digital or analog signals, for example as shown in Figure 1, where two signal lines A and B extend closely on the substrate 1, an abnormal voltage is so induced on either the signal line A or the signal line B by electrical capacitive coupling or inductive coupling between the signal lines A and B that a problem of electrical interference (i.e. cross talk) may occur.

For example as shown in Figure 1, electrical interference is liable to occur on the signal line B_0 transmitting a signal e_2 whose electrical amplitude is relatively small and which is disposed closely to the signal line A_0 transmitting a signal e_1 whose current- or voltage-amplitude is large and whose frequency is high.

In particular, in digital-analog hybrid circuits remarkable effects occur from a digital signal line to an analog line. As a result noise may be so generated on the analog signal line that the characteristic deteriorate or malfunction may occur. Such a mutual interference between digital signal lines may also cause the occurrence of a malfunction in digital circuits.

In order to prevent electrical interference between signal lines, attempts have been made to dispose these lines as far apart from each other as possible in the design lay-out on the substrate of the semiconductor integrated circuit. As a result, however, there is a problem that freedom in lay-out on the substrate of the semiconductor integrated circuit. As a result, however, there is problem that freedom in lay-out decreases or improvement of integration density on a semiconductor chip is prevented.

The present invention provides a semiconductor integrated circuit comprising:

a first signal line formed on a substrate of the semiconductor integrated circuit, arranged to transmit a first signal;

a second signal line formed on the substrate, arranged to transmit a second signal; and

a third signal line formed on the substrate, arranged to transmit a third signal of which the phase s opposite to that of the first signal so as to tend to cancel the cross talk between the first signal line and the second signal line by the cross talk between the second signal line and the third signal line.

Hereinafter the embodiments of the present invention will be explained with reference to the drawings, wherein:

Figure 1 is a plan view showing the layout of signal lines in a semiconductor integrated circuit according to the prior art;

Figure 2 is a plan view showing the layout of signal lines in a semiconductor integrated circuit according to one embodiment of the present invention;

Figure 3 is a plan view showing the layout of signal lines in a semiconductor integrated circuit according to another embodiment of the present invention;

Figure 4 is a plan view showing the layout of signal lines in a semiconductor integrated circuit according to another embodiment of the present invention;

Figure 5 is a plan view showing the layout of signal lines in a semiconductor integrated circuit according to another embodiment of the present invention;

Figure 6(A) and *6(B)* are a plan view and a cross-sectional view showing the structure of signal lines in a semiconductor integrated circuit according to the present invention;

Figure 7(A) and *(B)* are a plan view and a cross-sectional view showing the structure of signal lines in a semiconductor integrated circuit according to the present invention;

Figure 8(A) and *(B)* are a plan view and a cross-sectional view showing the structure of signal lines in a semiconductor integrated circuit according to the present invention;

Figure 9(A) and *(B)* are a plan view and a cross-sectional view showing the structure of signal lines in a semiconductor integrated circuit according to the present invention;

Figure 10(A) and *(B)* are a plan view and a cross-sectional view showing the structure of signal lines in a semiconductor integrated circuit according to the present invention;

Figure 11(A) and *(B)* are a plan view and a cross-sectional view showing the structure of signal lines in a semiconductor integrated circuit according to the present invention;

Figure 11(C) is a cross-sectional view showing the structure of signal lines in a semiconductor integrated circuit according to a modified embodiment of the present invention;

Figure 12(A) and *(B)* is a plan view and a cross-sectional view showing the structure of signal lines in a semiconductor integrated circuit according to the present invention; and

Figure 13(A) and *(B)* is a plan view and a cross-sectional view showing the structure of signal lines in a semiconductor integrated circuit according to the present invention.

In the semiconductor integrated circuits (IC) of the following embodiments only signal lines related to the present invention are illustrated and other circuits or circuit devices existing in the vicinity of these signal lines are omitted.

Figure 2 shows the lay-out of signal lines in a semiconductor integrated circuit according to an embodiment of the present invention.

In the embodiment of Figure 2 the third signal line A_2 which is parallel to the first signal line A_1 extends between the first signal line A_1 and the second signal line B_0. Signals of opposite phases are transmitted on the first signal line A_1 and the second signal line A_2 respectively. When signal line A_1 is disposed close to signal line A_2 and the distance between the signal line A_2 and the second signal line B_0 is approximately equal with the distance between the

signal line A_2 and the second signal line B_0 ($1_{A_1B_0} + 1_{A_2B_0}$), voltage or current fluctuations on the signal line B_0 induced by inductive coupling and capacitive coupling from the pair of signal lines A_1 and A_2 cancel each other because the phases of signals e_1 and $-e_1$ of the pair of signal lines A_1 and A_2 are opposite. As a result signal line B_0 can be saved from the influence of the first signal line A_1.

Figure 3 shows another embodiment. In the drawing there is disposed the third signal line A_2 transmitting signal $-e_1$ whose phase is opposite to that of the signal e_1 on the first signal line A_1. Signal lines A_1 and A_2 cross each other in a twisted fashion and signal currents e_1 and $-e_1$ whose phases are opposite each other flow into these signal lines A_1 and A_2. In this case by making them twisted the pair of signal lines A_1 and A_2 can be integrated more than in the case of the embodiment shown in Figure 2 and electrical interference on signal line B can be kept much smaller.

In contrast with the above, Figure 3 also illustrates the case where a strong signal current flows into the second signal line B and the second signal line B causes electrical interference on the first signal line A_1. By disposing signal lines A_1 and A_2 transmitting signals e_1 and $-e_1$ of opposite phases in close vicinity to the large current signal line B electric influences from signal line B become equal on the signal lines A_1 and A_2. When outputs of the pair of signal lines A_1 and A_2 are applied to double-end input terminals of a differential amplifier, the difference signals of the noise components at the output terminals of this differential amplifier becomes zero. As a result the noise can be removed. This structure shown in this embodiment is very effective in particular when a differential amplifier is disposed on the input side and differential outputs are extracted in double-end form.

Figure 4 shows an embodiment in which a differential amplifier 3 is disposed on the receiving side in order to prevent electrical interference or cross talk from the signal line B to a pair of signal lines A_1 and A_2 in the case where the second signal line B carries a signal current e_2 of relatively small electrical amplitude and the pair of signal lines A_1 and A_2 carry a pair of signal currents e_1 and $-e_1$. In the drawing, numeral 4 represents an input circuit disposed on signal line B. Numeral 5 represents an output circuit on signal line B. Numeral 2 represents a differential amplifier disposed on the input side of the pair of signal lines A_1 and A_2. Provision of a differential amplifier 3 on the receiving side (the output side of the pair of signal lines A_1 and A_2) enables common noises at the output terminal of the differential amplifier 3 to be removed by the common-mode rejection function of the differential amplifier 3 and electric effect from signal line B on signal lines A_1 and A_2 to be kept much smaller. This structure shown in Figure 4 is also effective in preventing electric interference from signal lines A_1 and A_2 to signal lines B.

Figure 5 shows an embodiment in which crossing the first and third signal lines in a twisted fashion produces a greater effect than in the embodiment shown in Figure 4. In Figure 5 the same reference numeral symbols as Figure 4 are used to denote similar parts.

Next the structure of the above mentioned signal lines A_1, A_2 and signal line B on the semiconductor substrate (chip) of the present invention will be explained as follows.

1. The embodiment of using a pair of parallel wirings A_1 and A_2 which carry signal currents of opposite phases for the purpose of transmitting the first signal e_1:

As shown in Figure 6(A) and (B) signal line B for transmitting the second signal e_2 and a pair of signal lines A_1 and A_2 which are made of Al (aluminum) films are respectively formed flat on the substrate 1 on an intermediate insulating film (SiO_3 film) 6.

The embodiment of Figure 7(A) and (B) shows that a pair of Al signal lines A_1 and A_2 are formed in double layers, one above the other, with an intermediate insulating film 7 (e.g. polyimide resin layer). The second signal line B is made of aluminum film on the same level as the lower aluminum film A_2.

In Figure 8(A) and (B), of a pair of signal lines A_1 and A_2 for the first signals the signal line A_1 is made of Al film and the other signal line A_2 is made of a semiconductor diffusion layer 8 the impurity conductivity type of which is different from that of the substrate and which is disposed in the surface of the semiconductor substrate 1 under the insulating film 6. Signal line B for the second signal e_2 is formed by an aluminum line in the same plane as signal line A_1.

In Figure 9(A) and (B) a pair of signal lines A_1 and A_2 of aluminum wirings for the first signals e_1 are formed on the insulating film 6 and a signal line B for the second signal e_2 is made of a semiconductor diffusion layer 9 the impurity conductivity type of which is different from that of the substrate and which is disposed in the surface of the semiconductor substrate 1 just below the signal lines A_1 and A_2.

In Figure 10(A) and (B) signal lines A_1 and A_2 of Al films for the first signals e_1 are formed in double layers one above the other with an intermediate insulating film 7. A signal line B for the second signal e_2 is made of a semiconductor diffusion layer 10 the impurity conductivity type of which is different from that of the substrate and which is disposed in the surface of the semiconductor substrate 1 just below the signal lines A_1 and A_2.

2. The embodiment using symmetric twisted lines A_1 and A_2 which carry the signal currents of opposite phases for the first signal e_1:

Figure 11(A), Figure 11(B) and Figure 11(C) show that in the signal lines A_1 and A_2 for the first signals e_1 the signal line A_1 is made of Al film formed on the substrate over an insulating film 6, and the signal line A_2 is made of a semiconductor diffusion layer 8 the impurity conductivity type of which is different from that of the substrate and which is formed on the surface of the semiconductor substrate below the insulating film 6. The signal lines A_1 and A_2 cross and recross each other symmetrically when viewed in plan as shown in Figure 11(A). The second signal line B is made of Al film in the same plane as the signal line A_1.

Figure 11(C) shows a modified embodiment of Figure 11(B). In the drawing signal lines A_1 and A_2 for

the first signals e_1 are formed by Al films in upper and lower layers which are isolated from each other by intermediate insulating film 7, and both of them are wired in twist form when viewed in plan as shown in Figure 11(A).

Figure 12(A) and Figure 12(B) show the following structure.

Namely, a pair of signal lines A_1 and A_2 for the first signals is made of Al films and wired in twist form on the surface of the insulating film 6. At the crossing part of the signal lines A_1 and A_2 a part of the signal line A_2 are connected by Al upper layer 12 which is bridging a pair of through-holes 11 formed in the intermediate insulating film 7. Thus, the signal lines A_1 and A_2 cross each other in electrically isolated condition.

Figure 13(A) and Figure 13(B) show the following structure.

Namely, a pair of signal lines A_1 and A_2 for the first signals is made of Al films and wired in twist form on the surface. At the crossing part of he signal lines A_1 and A_2 a part of one signal line (e.g. the signal line A_2) is cut off. Along this cut-off part of the signal line A_2 the impurity diffusion layer 13 the conductivity type of which is different from that of the substrate is formed on the surface of the semiconductor substrate 1. Parts of Al films of the signal line A_2 are brought into contact with the diffusion layer 13 through the through-holes 14 which are formed in the insulating film 6. Thus, the signal lines A_1 and A_2 cross each other in electrically isolated condition.

According to the embodiments described above noise which is generated by electric interference between signal lines in the semiconductor integrated circuit can be removed by using a pair of signal lines of opposite phases or a pair of signal lines of twist-symmetrical configuration configuration, or provided with a differential amplifier.

As a result, freedom in layout and easy circuit design can be achieved and integration density is improved.

The present invention may be applied to digital circuits, analog circuits and semiconductor integrated circuits combining the above-mentioned circuits.

CLAIMS

1. A semiconductor integrated circuit comprising:

a first signal line formed on a substrate of the semiconductor integrated circuit, arranged to transmit a first signal;

a second signal line formed on the substrate, arranged to transmit a second signal; and

a third signal line formed on the substrate, arranged to transmit a third signal of which the phase is opposite to that of the first signal so as to tend to cancel the cross talk between the first signal line and the second signal line by the cross talk between the second signal line and the third signal line.

2. A semiconductor integrated circuit according to claim 1, wherein the effective distance between the first signal line and the second signal line is substantially equal with the effective distance between the second signal line and the third signal line.

3. A semiconductor integrated circuit according to claim 2, wherein the first signal line and the third signal line cross each other in a symmetric configuration.

4. A semiconductor integrated circuit according to claim 2 or claim 3 wherein the first and third signal lines are in a symmetric twisted configuration.

5. A semiconductor integrated circuit according to any one of claims 1 to 4, further comprising a differential amplifier of which differential input terminals receive the first signal and the third signal.

6. A semiconductor integrated circuit according to claim 5, wherein the differential amplifier has a common-mode rejection function with respect to the differential input terminals.

7. A semiconductor integrated circuit according to claim 5 or claim 6, further comprising another differential amplifier of which output terminals deliver the first signal and the third signal to the first signal line and the third signal line.

8. A semiconductor integrated circuit substantially as any described herein with reference to Figures 2 to 13 of the accompanying drawings.

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